

PCT

WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

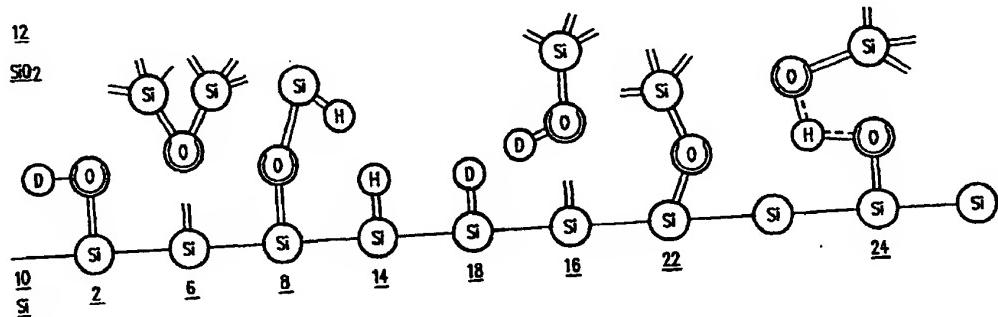


INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 5 :	A1	(11) International Publication Number: WO 94/19829
H01L 29/40, 21/306		(43) International Publication Date: 1 September 1994 (01.09.94)

(21) International Application Number: PCT/US94/01669	(81) Designated States: JP, KR, European patent (AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).
(22) International Filing Date: 17 February 1994 (17.02.94)	Published <i>With international search report. Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.</i>
(30) Priority Data: 08/019,934 19 February 1993 (19.02.93) US	
(71) Applicant: NATIONAL SEMICONDUCTOR CORPORATION [US/US]; 2900 Semiconductor Corporation, Santa Clara, CA 95052-8090 (US).	
(72) Inventors: LISENKER, Boris, S.; 4/53 Nissenbaum, Haifa 04 (IL). JANKELEVICH, Alfred; 14 Hillel, Haifa 04 (IL).	
(74) Agent: RODDY, Richard, J.; National Semiconductor Corporation, 2900 Semiconductor Drive, M/S 16-135, Santa Clara, CA 95052-8090 (US).	

(54) Title: SEMICONDUCTOR DEVICE COMPRISING DEUTERIUM ATOMS



(57) Abstract

A method is provided in which a silicon wafer is contacted with a deuterium containing material to form Si-D and Si-OD bonds on a silicon surface at an interface with a silicon dioxide layer. An MOS device is formed by employing deuterium containing compounds at various stages of the fabrication procedure. After an MOS gate oxide is formed, the wafer is annealed in a deuterium containing atmosphere and a polysilicon layer is formed by chemical vapor deposition employing deuterium containing compounds. The device is subsequently cleaned with a deuterium containing compound such as D₂O, D₂SO₄, and DCl.

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AT	Austria	GB	United Kingdom	MR	Mauritania
AU	Australia	GE	Georgia	MW	Malawi
BB	Barbados	GN	Guinea	NE	Niger
BE	Belgium	GR	Greece	NL	Netherlands
BF	Burkina Faso	HU	Hungary	NO	Norway
BG	Bulgaria	IE	Ireland	NZ	New Zealand
BJ	Benin	IT	Italy	PL	Poland
BR	Brazil	JP	Japan	PT	Portugal
BY	Belarus	KE	Kenya	RO	Romania
CA	Canada	KG	Kyrgyzstan	RU	Russian Federation
CF	Central African Republic	KP	Democratic People's Republic of Korea	SD	Sudan
CG	Congo	KR	Republic of Korea	SE	Sweden
CH	Switzerland	KZ	Kazakhstan	SI	Slovenia
CI	Côte d'Ivoire	LI	Liechtenstein	SK	Slovakia
CM	Cameroon	LK	Sri Lanka	SN	Senegal
CN	China	LU	Luxembourg	TD	Chad
CS	Czechoslovakia	LV	Latvia	TG	Togo
CZ	Czech Republic	MC	Monaco	TJ	Tajikistan
DE	Germany	MD	Republic of Moldova	TT	Trinidad and Tobago
DK	Denmark	MG	Madagascar	UA	Ukraine
ES	Spain	ML	Mali	US	United States of America
FI	Finland	MN	Mongolia	UZ	Uzbekistan
FR	France			VN	Viet Nam
GA	Gabon				

SEMICONDUCTOR DEVICE COMPRISING DEUTERIUM ATOMS

BACKGROUND OF THE INVENTION

The present invention relates to silicon-based electronic devices and methods of fabricating them. In particular, the present invention provides improved VLSI fabrication methods that minimize some of the detrimental effects associated with hydrogen in oxides.

Oxide layers are used to isolate devices and device elements on an integrated circuit. They are also used to control leakage currents in junction devices and act as stable gate oxides in field effect devices.

Many semiconductor device elements rely on high quality silicon dioxide layers and the bonds they provide with adjacent surfaces. For example, high quality gate oxide layers are critical to the performance of MOSFET devices. Unfortunately, the performance of many silicon devices is limited by the oxide layer and the quality of the interface it provides with adjacent surfaces. In MOS devices, the problematic interfaces include the gate conductor (usually polysilicon)-gate oxide interfaces as well as the gate oxide-semiconductor interface. See Sah, Solid-State Electronics (1990) 33:147-167, incorporated herein by reference for all purposes.

Poor quality oxide is evidenced by such effects as unstable threshold voltages in MOS devices, leakage currents at junctions, high 1/f noise, high sensitivity to hot carrier degradation, high sensitivity to ESD (Electrical Static Discharge) or EOS (Electrical Over Stress), irradiation immunity, etc. These problems can result from a variety of physical factors, including increased numbers of surface states (at the silicon surfaces) caused by uncompleted or "dangling" silicon bonds, increased fixed charge on the silicon/silicon dioxide interface, and

WO 94/19829

2

vacancies in the bulk oxide. The increased number of surface states can be populated by electrons that impose a potential on the silica/silicon interface. The fixed charge also contributes to the electrical fields at the interface. If the fixed charge and surface state densities become too great, the threshold voltage required for circuit operation becomes impractical.

An important property of high quality silicon dioxide is its ability to reduce the surface state density of silicon by tying up some of the dangling bonds. In addition, high quality silicon dioxide should provide good control over interface traps and fixed charge.

Unfortunately, even the best oxide layers leave a large number of dangling bonds at the silicon-oxide interfaces.

Some of these bonds can be completed by annealing the oxidized silicon wafer in hydrogen or a mixture of hydrogen and nitrogen. For example, wafers are sometimes heated in hydrogen at 450°C for approximately 15 minutes to form silicon-hydrogen (Si-H) bonds at the interface, thus reducing the density of surface states. A detailed discussion of the role hydrogen plays in failure mechanisms is provided in the review by C.T. Sah, "Models and Experiments on Degradation of Oxidized Silicon", Solid-State Electronics (1990) 33:147-167, previously incorporated by reference.

Hydrogen can also be introduced unintentionally by a variety of standard fabrication processes including thermal oxidation of the wafer, post-oxidation treatments of the wafer, and ambient oxidation of the silicon surface. All of these processes result in the formation of Si-H and Si-OH bonds. A detailed discussion of the sources of hydrogen in silica films on silicon is provided in Revesz, J. Electrochem. Soc. (1979) 126:122-130, which is incorporated herein by reference for all purposes.

Some hydrogen is introduced in the form of water present in materials used to fabricate semiconductor devices. In wet thermal oxidation processes water is

WO 94/19829

3

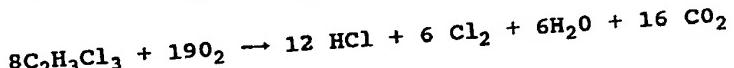
purposely employed to form oxides, usually isolation oxides. These processes are rapid, but result in a somewhat porous oxide film. The detailed nature of the reaction of silicon with water vapor to form silica is somewhat complex and described in S. Gandhi, *VLSI Fabrication Principles, Silicon and Gallium Arsenide*, John Wiley & Sons (1983), chpr. 7, which is incorporated herein by reference for all purposes.

5

Higher quality gate oxides in MOS devices may be formed by a "dry" oxygen process in which water is purposely excluded. Even so, some "contaminating" water is usually present, resulting in the formation of Si-H and Si-OH bonds. For example, a commonly used process of forming gate oxide employs trichloroethane at 900°C (near the wafer surface) according to the following reaction:

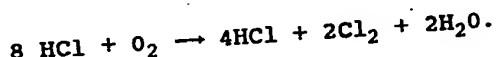
10

15



20

Hydrogen chloride gas reacts under comparable conditions as follows:



25

As seen, these processes produce water as a byproduct. Hydrogen can also be introduced by deposition of polysilicon from SiH_4 or another silane. Even cleaning with hydrogen-containing agents such as water, hydrochloric acid, and sulfuric acid can introduce hydrogen. Finally, oxidation of silicon surfaces by simple exposure to ambient conditions produces an oxide layer containing hydrogen.

30

As noted above the introduction of hydrogen has the beneficial result of tying up some dangling bonds at the silicon/silica interface. Unfortunately, the resulting Si-H bonds (as well as other compensating bonds such as Si-OH) are weaker than Si-O bonds formed with the bulk oxide layer. During electrical stresses, the density of silicon dangling bonding is increased because Si-H and Si-OH bonds break and

35

WO 94/19829

4

the resulting hydrogen species migrate away.

One source of such electrical stress is electrons having energies over 3.2eV which surmount the barrier between silicon and silicon dioxide. These "hot" electrons (or the resulting holes) can become trapped in the silica layer and break some of the silicon-hydrogen and silicon-OH bonds at the silicon and silicon dioxide interface. Hot electrons are especially prevalent during avalanche breakdown of a P-N junction, since the energy of avalanching carriers has a mean value of about 3eV. Hot electrons can also be produced in the channel region of MOS transistors, resulting in a change in the threshold voltage.

Higher quality silicon dioxide layers having reduced numbers of dangling and/or weak Si-H bonds are needed to improve the performance of many semiconductor devices. A concomitant new method of fabricating such silicon dioxide layers is likewise needed.

SUMMARY OF THE INVENTION

The present invention provides a method in which a silicon wafer is contacted with a deuterium containing material to form Si-D and Si-OD bonds in a silicon dioxide layer and on a silicon surface at an interface with the silicon dioxide layer. Typical silicon dioxide layers suitable for treatment according to the present invention include isolation oxides, gate oxides, and various other oxide layers commonly used with semiconductor devices. According to the invention, deuterium or a deuterium-containing material is directed onto the device by, for example, annealing in a deuterium containing atmosphere, and/or cleaning with a deuterium compound such as D₂O, D₂SO₄, and DCl. In general, any hydrogen containing material used in VLSI fabrication can be replaced with corresponding deuterium containing material.

The stability of oxide layers is improved in the present invention because the bond energy of the Si-H and Si-OH bonds is increased by replacing the hydrogen atoms

WO 94/19829

5

with deuterium atoms. The Si-D and Si-OD bonds thus formed provide completed silicon dangling bonds that are less likely to break when exposed to electrical stresses. Therefore, the deuterium containing devices of the present invention have improved stability, quality, and reliability.

5

10

In one aspect of the present invention, VLSI fabrication flows employ deuterium contained compounds in many or all of the fabrication steps that would normally employ hydrogen or a hydrogen containing compound. Thus, for example, a wet thermal oxidation step is performed with heavy water rather than normal water, an annealing step is conducted in a deuterium atmosphere rather than a hydrogen atmosphere, a polysilicon chemical vapor deposition step is performed with SiD_4 rather than silane, etc.

15

Devices of this invention will preferably have substantial numbers of Si-H and/or Si-OH bonds replaced with Si-D and/or Si-OD bonds. Deuterium atoms represent a very small fraction of the atoms in naturally occurring hydrogen. In preferred embodiments of this invention the ratio of deuterated to hydrogenated silicon bonds is substantially greater than the naturally occurring fraction of deuterium atoms. In most preferred embodiments the ratio of Si-D plus Si-OD bond to Si-H plus Si-OH bonds in the oxide and oxide-silicon interfaces will be greater than about 95:5.

20

A further understanding of the nature and advantages of the invention herein may be realized by reference to the remaining portions of the specification and the attached drawing.

25

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a representation of a silicon-silicon dioxide interface having some desirable features of the present invention.

30

DESCRIPTION OF THE SPECIFIC EMBODIMENTS

The present invention provides a method for producing semiconductor devices in which hydrogen-containing

35

WO 94/19829

6

bonds in silicon dioxide are replaced with deuterium containing bonds. Specifically Si-H bonds are replaced with Si-D bonds and Si-OH bonds are replaced with Si-OD bonds. Because the deuterium containing bonds are less likely to break on exposure to electrical stresses, devices prepared according to this invention have various advantages over conventional devices. For example, they have more stable gate threshold voltage in MOS devices and better control over leakage currents in junction devices.

The formation of Si-D and Si-OD bonds is accomplished in the present invention by contacting a silicon wafer with deuterium or a deuterium containing compound before, during, and/or after formation a device oxide layer. As used herein, the expression "deuterium" refers to materials that include deuterium in a concentration above its naturally occurring level. Thus, for example, pure gaseous D₂ as well as a gaseous mixture of 50% H₂ and 50% D₂ qualify as "deuterium." In fact, any artificial gaseous mixture containing a ratio of D₂ to H₂ above the naturally occurring level constitutes "deuterium" as used herein. The naturally occurring concentration of deuterium is about one part in 6000 parts of hydrogen.

The expression "deuterium containing compound" is intended to refer to compositions containing deuterated compounds in a concentration above the naturally occurring level. Thus, a solution of 50% D₂O in H₂O would constitute a deuterium containing compound. Likewise, compositions containing DCl, D₂SO₄, SiD₄ are "deuterium containing compounds" so long as the deuterium containing compounds are present at a concentration greater than that of naturally occurring deuterium in hydrogen.

Referring now to Fig. 1, an interface region between a silicon layer 10 and a silicon dioxide layer 12 is schematically represented. Silicon layer 10 may be, for example, a highly doped, conductive polysilicon gate contact or a single crystal silicon semiconductor. The bulk oxide layer consists of infinitely linked SiO₄ tetrahedra with an

WO 94/19829

7

occasional oxygen vacancy or other fault. Ideally, all silicon atoms at the interface are bonded to an oxygen atom associated with the oxide network. For example, at positions 8 and 22, silicon atoms on the surface of the silicon layer are bonded to oxygen atoms that are incorporated into SiO_4 tetrahedra. However, not all surface silicon atoms are bonded with the oxide layer. For example, at positions 6 and 16, surface silicon atoms are displayed with dangling bonds. These situations are undesired because of the extra surface states associated with uncompleted silicon bonds. At position 6, the oxide layer oxygen atom nearest to the silicon surface is incorporated into two SiO_4 tetrahedra, while at position 16, the nearest oxygen atom is incorporated into one SiO_4 tetrahedra and bonded to one deuterium atom.

Some silicon atoms at the interface have completed bonds with species other than the SiO_4 tetrahedra of the bulk oxide. These bonding arrangements include Si-H and Si-OH groups shown at positions 14 and 24, respectively. As noted, these bonds result from contact of hydrogen or hydrogen containing compounds during the device fabrication steps. Some of them may have even been formed intentionally by hydrogen annealing to saturate dangling silicon bonds. The bonding arrangements shown at positions 2 and 18 are favored for the present invention. At these positions, silicon atoms that would otherwise have dangling bonds are saturated by coupling with -OD and -D. These bonds are less likely than their hydrogen counterparts to break when subjected to electrical stresses.

As shown below, the zero-point energy levels of deuterium containing bonds are lower than the corresponding hydrogen containing bonds and hence need a greater thermodynamic driving force to break them.

35	Si-H - 71.5 Kcal/mole O-H - 102.2 Kcal/mole	Si-D - 72.3 Kcal/mole, O-D - 104.3 Kcal/mole.
----	--	--

(See, CRC Handbook of Chemistry and Physics, 64th edition,

WO 94/19829

8

1983-1984; CRC Press Incorporation, Boca Raton, Florida, P
F176-179.)

Further, the kinetic isotope effect in the
chemical reactions requires that deuterium containing bonds
break more slowly than the corresponding hydrogen containing
bonds. The rate constant of chemical reactions involving
important deuterium-containing molecules (K_d) is smaller
than for hydrogen-containing molecules (K_h) as shown.

10 $K_d/K_h = 0.75 - 0.85$ for triphenylsilane,
 $K_d/K_h = 0.4$ for chloroform,
 $K_d/K_h = 0.5$ for chloride.

15 (See, L. Melander, Isotope Effects on Reaction Rates, The
Ronald Press Company, N.Y., 1960, which is incorporated
herein by reference for all purposes)

20 In addition, the ionic product of D_2O (i.e.
 $[D^+][OD^-]$) is smaller by about an order of magnitude than the
corresponding ionic product of H_2O . Thus, fewer reactive
ions are present in heavy water than in normal water. By
replacing normal water with heavy water in processing steps
such as thermal oxide formation and cleaning, the potential
for chemical reaction on oxide surface is decreased. The
ion product constant of D_2O is 1.1×10^{-15} while the ion
product constant for H_2O is 1.01×10^{-14} . (See, Isotope Effects
in Chemical Reactions, Edited by C.J. Collins and S. Barman,
Van Nostrand Reinhold Company, N.Y., 1970, which is
incorporated herein by reference for all purposes).

25 The present invention can be implemented
30 throughout the VLSI fabrication procedure. A typical
fabrication procedure will include various doping, etching,
annealing, deposition, cleaning, passivation, and oxidation
steps. In each instance in which hydrogen or a hydrogen
containing compound is employed, deuterium or a deuterium
containing compound can be used in its place. This is
35 particularly important in those fabrication steps in which a
permanent oxide layer is being formed or treated. The
method of this invention can be implemented, for example, by

WO 94/19829

9

annealing in N₂ ambient with D₂, by replacing HCl and/or H₂O with DCl and/or D₂O during cleaning, or by using deuterium containing compounds during chemical vapor deposition to form polysilicon layers.

Preferably, deuterium or deuterium containing compounds having a mole fraction of near 1 (for the deuterated versions) are employed in fabrication steps. However, lower concentrations of deuterated compounds may also be employed, but generally require a longer reaction or contact time to ensure formation of a substantial percentage of Si-D and/or Si-OD bonds. Because deuterated bonds are more stable than their hydrogen-containing counterparts, they ultimately supplant some hydrogenated bonds during long exposure to deuterium containing compounds.

Preferred annealing atmospheres of the present invention includes a deuterium mole fraction of greater than about 0.90, and more preferably greater than about 0.95. In especially preferred embodiments, the annealing atmosphere includes a deuterium mole fraction of greater than about 0.99. The deuterium containing annealing atmosphere is preferably provided at a temperature of about 500°C and a pressure of about one atmosphere. These conditions are typically maintained for approximately 10 to 20 minutes. Of course, other acceptable conditions will be apparent to those of skill in the art.

During cleaning of silicon wafers, some molecules of the cleaning agent are incorporated into the device structure. If the cleaning agent includes hydrogen in its molecular structure, some Si-H and Si-OH bonds form. To promote formation of deuterium containing bonds over hydrogen containing bonds, the semiconductor devices fabricated according to the present invention are preferably cleaned with a deuterium containing compound. Thus, preferred cleaning compounds include D₂O, D₂SO₄, CDCl₃, and DCl. Of course, any other common hydrogen containing cleaning compound can be replaced with the corresponding deuterium containing compound.

WO 94/19829

10

Wet thermal oxidation of the silicon wafer can be conducted using heavy water. A suitable process is conducted by bubbling a carrier gas such as oxygen, nitrogen, or argon through a heavy water bath. Some of the heavy water will be vaporized in the process and transported with the carrier gas to the silicon surface where an oxide layer is formed. In some alternative thermal oxidation methods, deuterium and oxygen gases are passed through a diffusion tube to form heavy water that is used to produce the oxide film. In either method, some of the deuterium atoms from the heavy water will bond with surface silicon atoms. Although such bonds are less preferred than Si-O bonds with the bulk oxide, they are an inevitable side product of any wet oxidation processes. Because heavy - rather than normal - water is employed, these less preferred bonds will be satisfied with deuterium or deuterium oxide groups.

The use of silanes such as SiH_4 and $\text{Si}(\text{C}_6\text{H}_5)_3\text{H}$ during chemical vapor deposition steps is another source of hydrogen in normal VLSI fabrication procedures. If deuterated silanes are substituted for their hydrogen counterparts, the density of Si-H and Si-OH bonds will be further reduced. In general, any of the organosilicon compounds widely used in VLSI technology can be replaced with the corresponding deuterium analogs.

In general, electronic devices formed according to the above processes will have an increased number of Si-OD and Si-D bonds in comparison with devices formed using conventional processes. The regions where the deuterated bonds provide the greatest benefit in terms of device performance is at the interface of silicon-silicon dioxide layers. Thus, the semiconductor devices of this invention will have at this interface a ratio of Si-OD plus Si-D bonds to Si-OH plus Si-H bonds that is substantially greater than ratio of naturally occurring deuterium to hydrogen. Similar ratios will be found in the bulk oxide of the devices. Thus, the ratio will be substantially greater than 1:6000

WO 94/19829

11

deuterated to hydrogenated bonds at the interface and in the bulk oxide. In preferred embodiments, the ratio of deuterated to hydrogenated silicon bonds will be greater than about 95:5, and in more preferred embodiments, greater than about 99:1. Especially preferred devices of this invention are MOS transistors in which the gate oxide-silicon layer contains additional deuterium containing bonds. However, other devices such as bipolar junction transistors are also within the purview of this invention.

5 It is to be understood that the above description is intended to be illustrative and not restrictive. Many variations of the invention will become apparent to those of skill in the art upon review of this disclosure. For example, while the invention has been illustrated with regard to specific deuterium containing compounds, it should be clear that a wide variety of deuterium containing compounds may be used herein without departing from the scope of the inventions herein. The scope of the invention should, therefore be determined not with reference to the above description, but instead should be determined with reference to the appended claims along with their full scope of equivalents.

10

15

20

WHAT IS CLAIMED IS:

1. A semiconductor device comprising at least one silicon dioxide layer and an interface between the silicon dioxide layer and a silicon surface, the silicon dioxide layer and the interface having Si-OD and Si-D bonds; wherein the ratio of Si-OD plus Si-D bonds to Si-OH plus Si-H bonds is substantially greater than ratio of naturally occurring deuterium to hydrogen.
2. The semiconductor device of claim 1 wherein the ratio of Si-OD plus Si-D bonds to Si-OH plus Si-H bonds is greater than about 95:5.
3. The semiconductor device of claim 2 wherein the ratio of Si-OD plus Si-D bonds to Si-OH plus Si-H bonds is greater than about 99:1.
4. The semiconductor device of claim 1 wherein the silicon surface is on a conductive polysilicon gate contact of an MOS device.
5. An MOS device comprising a gate oxide including silicon dioxide and an interface between the gate oxide and a silicon surface, the silicon dioxide and the interface having Si-OD and Si-D bonds; wherein the ratio of Si-OD plus Si-D bonds to Si-OH plus Si-H bonds is substantially greater than ratio of naturally occurring deuterium to hydrogen.
6. The MOS device of claim 5 wherein the ratio of Si-OD plus Si-D bonds to Si-OH plus Si-H bonds is greater than about 95:5.
7. The MOS device of claim 6 wherein the ratio of Si-OD plus Si-D bonds to Si-OH plus Si-H bonds is greater than about 99.1.

WO 94/19829

13

8. The MOS device of claim 5 wherein the silicon surface is on a conductive polysilicon gate contact.

5 9. The MOS device of claim 5 wherein the silicon surface is on a semiconducting silicon surface.

10 10. A method of fabricating a semiconductor device containing at least one silicon dioxide layer and a silicon surface having an interface with the silicon dioxide layer, the method comprising:
directing a deuterium containing compound onto a silicon wafer; and forming Si-D bonds at the silicon and silicon dioxide interface.

15 11. The method of claim 10 wherein the step of contacting is a cleaning operation and wherein the deuterium containing compound is a cleaning agent selected from the group consisting of DCI, D₂SO₄, CDCl₃, and D₂O.

20 12. The method of claim 10 further comprising a step of forming a gate oxide.

25 13. The method of claim 10 wherein the step of contacting the silicon wafer is a thermal oxidation step, and the deuterium containing compound is heavy water vapor, D₂O.

30 14. The method of claim 10 wherein the step of contacting the silicon wafer with a deuterium containing compound is an annealing step, and the deuterium containing compound is deuterium gas.

35 15. The method of claim 10 wherein the step of contacting the silicon wafer with a deuterium containing compound is a chemical vapor deposition step.

16. A method of fabricating a silicon semiconductor device, the method comprising annealing the semiconductor wafer in an annealing atmosphere including deuterium.

5

17. The method of claim 16 wherein the annealing atmosphere includes deuterium mole fraction of at least about 0.95.

10

18. The method of claim 16 wherein the annealing atmosphere includes nitrogen.

15

19. The method of claim 16 further comprising steps of forming a silicon dioxide layer and doping the semiconductor wafer.

20

20. The method of claim 16 wherein the atmosphere is substantially free of hydrogen.

25

21. A method of cleaning a semiconductor device, the method comprising contacting a silicon wafer containing at least one silicon dioxide layer with a deuterium containing cleaning compound.

30

22. The method of claim 21 further comprising the steps of doping the silicon wafer and annealing the wafer in an atmosphere including deuterium gas.

23. The method of claim 21 further comprising a step of forming a gate oxide.

35

24. The method of claim 21 wherein the deuterium containing cleaning compound is selected from the group consisting of D₂O, D₂SO₄, CDCl₃, and DCI.

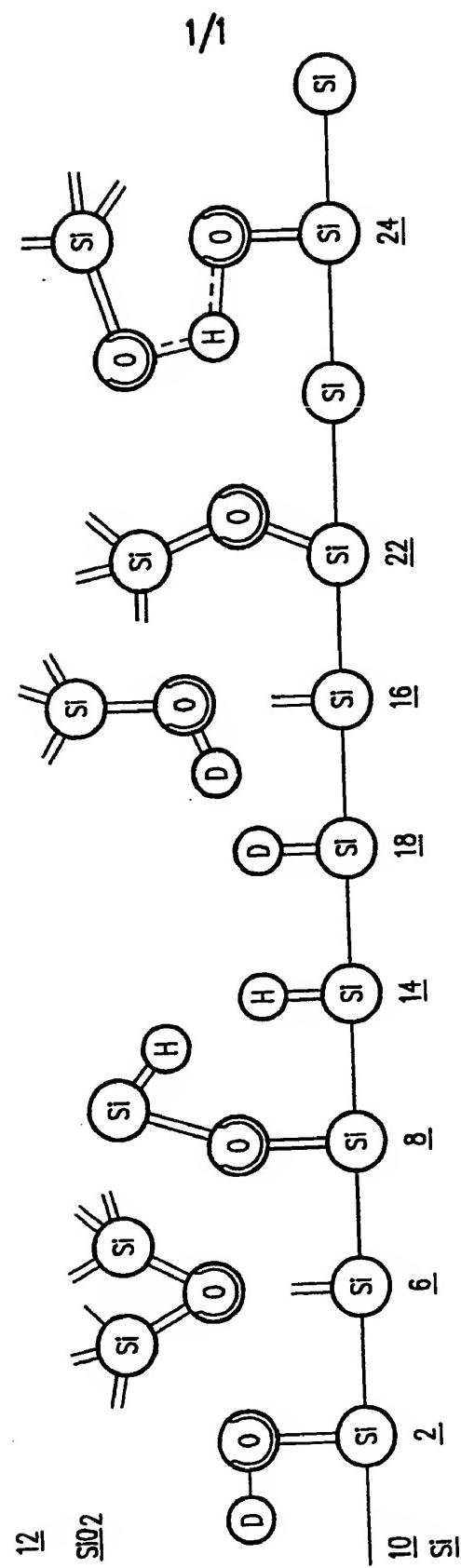


FIG. 1

SUBSTITUTE SHEET (RULE 26)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 94/01669

A. CLASSIFICATION OF SUBJECT MATTER
IPC 5 H01L29/40 H01L21/306

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 5 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	JOURNAL OF ELECTRONIC MATERIALS vol. 11, no. 3 , 1982 , USA pages 541 - 558 J.C. MIKKELSEN JR. 'SECONDARY ION MASS SPECTROMETRY CHARACTERIZATION OF D2O AND H2 18O STEAM OXIDATION OF SILICON' see page 541, line 13 - page 546, line 2 ---	1-13
X	JOURNAL OF THE ELECTROCHEMICAL SOCIETY vol. 139, no. 7 , July 1992 , MANCHESTER, NEW HAMPSHIRE US pages 2042 - 2046 H. PARK ET AL. 'THE EFFECT OF ANNEALING TREATMENT ON THE DISTRIBUTION OF DEUTERIUM IN SILICON AND IN SILICON/SILICON OXIDE SYSTEMS' see the whole document ---	1,5,10, 13,14, 16,18

Further documents are listed in the continuation of box C.

Patent family members are listed in annex.

* Special categories of cited documents :

- 'A' document defining the general state of the art which is not considered to be of particular relevance
- 'E' earlier document but published on or after the international filing date
- 'L' document which may throw doubt on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
- 'O' document referring to an oral disclosure, use, exhibition or other means
- 'P' document published prior to the international filing date but later than the priority date claimed

'T' later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

'X' document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

'Y' document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

'&' document member of the same patent family

Date of the actual completion of the international search

Date of mailing of the international search report

29.06.94

20 June 1994

Name and mailing address of the ISA
European Patent Office, P.B. 5818 Patentaan 2
NL - 2280 HV Rijswijk
Tel. (+ 31-70) 340-2040, Tx. 31 651 epo nl
Fax (+ 31-70) 340-3016

Authorized officer

Baillet, B

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 94/01669

C(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT		Relevant to claim No.
Category	Citation of document, with indication, where appropriate, of the relevant passages	
X	RADIATIONS EFFECTS AND DEFECTS IN SOLIDS vol. 111-112, no. 1-2 , 1989 , UK page 299-308 G.S. OEHRELEIN ET AL. 'SECONDARY ION MASS SPECTROMETRY MEASUREMENTS OF DEUTERIUM PENETRATION INTO SILICON BY LOW PRESSURE RF GLOW DISCHARGES' see paragraph II ---	1,5, 8-12,14
X	APPLIED PHYSICS LETTERS vol. 61, no. 25 , 21 December 1992 , NEW YORK US pages 3014 - 3016 N.S. SAKS ET AL. 'TIME-DEPENDENCE OF THE INTERFACE TRAP BUILD-UP IN DEUTERIUM-ANNEALED OXIDES AFTER IRRADIATION' see the whole document ---	1,5,10, 14,16
X	JOURNAL OF APPLIED PHYSICS vol. 67, no. 9 , 1 May 1990 , NEW YORK US pages 4064 - 4071 S.M. MYERS ET AL. 'INTERACTIONS OF DEUTERIUM WITH ION-IRRADIATED SiO ₂ ON Si' see page 4064 - page 4065 -----	1,4, 8-10,16, 17,20
X	PATENT ABSTRACTS OF JAPAN vol. 14, no. 520 (E-1002)14 November 1990 & JP,A,02 218 128 (FUJITSU LTD) 30 August 1990 see abstract -----	21